Clean Version of Changes to Specification

Please replace the paragraph at page 7, lines 1-7 with the following paragraph.

It is another object of the present invention to provide a method for making a heterojunction bipolar transistor which performs low termal-cycle processing, which, in turn, allows the present method to use thin low-temperature epitaxy (LTE) layers in the formation of base and collector regions. Use of thin LTE layers for these regions increases speed of the transistor and, further, leads to a lowering of the overall topography of the device, making mid-end-of-line (MEOFL) processed such as emitter, base, and collector contact opening much easier.

Please replace the paragraph at page 4, lines 1-10 with the following paragraph.

In Figure 1(h), a collector pedestal implant 20 for a high f_T device is formed beneath the p-type SiGe base in n^- region 5. Implant 20 is self-aligned to the emitter opening and extrinsic base implant regions and is an n-type implant. (The variable f_T is the cutoff frequency of the transistor and is an important figure of merit for high-frequency and microwave transistors. It is defined as the frequency at which the common emitter short-circuit current gain is unity. The cutoff frequency is inversely proportional to the total emitter-to-collector delay time t_{ec}. As a figure of merit, it is indicative of the raw speed at which device is capable of operating. To obtain a higher f_T, the transistor should have a very narrow base, a very narrow collector, and low capacitances.)